7/9/03

REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants would like to thank the Examiner for allowing claim 40 and for indicating that claims 7-12, 14, and 16-17, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 7-12, 14, 15, and 20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim Applicants' subject matter due to a typographical error with reference to claim 2. Applicants have corrected the typographical error in claim 2.

Claims 1-6, 13, 15, and 18-39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,141,021 (Bickford et al.).

BICKFORD FAILS TO DESCRIBE A FIRST INTERNAL SIGNAL PATH AND A FIRST EXTERNAL SIGNAL PATH

Firstly, according to the Office Action, the claimed first internal signal path corresponds to the path connecting structures 118 and 110, and the claimed first external path corresponds to the path connecting structures 110 and 120 as shown in Figure 3. However, the path connecting structures 118 and 110, and the path connecting structures 110 and 120 are the same path, namely AGP 110, as also shown in Figure 3. Unlike the claims, these paths in Bickford are not separate paths, but the same path, as acknowledged in the Office Action as AGP 110. The Office Action also uses AGP 110 to describe the internal and external paths (referring to structures 118 and **110**, and **110** and 120). However, the claims require separate paths, namely a first internal signal path and a first external signal path where the input buffer is operable to receive the first external signal via the first external signal path. Accordingly, the first internal signal path is distinct from the first external signal path.

As to claim 1, for example, Applicants claim a first internal circuit, such as an internal bus bridge or internal graphics processor, that provides a first internal signal via an internal signal path. An input buffer is operable to receive a first external signal, such as from an

external graphics processor, via an external signal path. A selector circuit is coupled to both the first internal circuit and to the input buffer. The selector circuit is coupled to the first internal circuit via the internal signal path and is operable to select either the first internal signal or the external signal to provide as a selected signal. As such, among other advantages, the input buffer isolates the external signal path from the first internal circuit. No such input buffer, first external path, or selector circuit as arranged in the claims is taught or suggested by the cited reference and as such, the rejection is improper.

Secondly, Bickford teaches the use of a conventional bus architecture so that "devices on the bus can send and receive information from other devices." (Bickford Col. 1, lines 19-20). Accordingly, a motherboard includes an AGP graphics accelerator chip 118 coupled to the accelerated graphics port (AGP) 110. (Bickford Col. 4, lines 41-44). Bickford also requires a connector 120 coupled to the AGP 110 that is adapted to receive an AGP graphics accelerator add-in card 122. As a result, Bickford does not teach a first external signal path because Bickford teaches, "A connector 120 adapted to receive an AGP graphics accelerator add-in card 122 is coupled to the AGP 110, along with a device 124 for selectively disabling either on board AGP graphics accelerator 118 or the add-in AGP card seated 122 in the connector 120." Therefore, unlike the claims, Bickford teaches that the same AGP 100 is coupled to both the on board AGP graphics accelerator chip 118 and to the add-in card 122. As previously stated, the claims require separate paths, namely a first internal signal path and a first external signal path where the input buffer is operable to receive the first external signal via the first external signal path. As a result, since the connector 120 is directly coupled to the AGP, Bickford does not teach and further teaches against a first external path. Consequently, Bickford teaches against a first internal signal path and a first external signal path where the input buffer is operable to receive the first external signal via the first external signal path. Therefore, since Bickford as cited teaches against the claims, the Office Action fails to establish a *prima facie* case of obviousness.

Thirdly, the Office Action acknowledges that Bickford fails to teach an input buffer. Rather than teaching an input buffer is operable to receive the first external signal via the first external signal path, Bickford is directed to merely disabling and enabling AGP graphics accelerators 118, 122 coupled to the same AGP 110 (Bickford Col. 4, lines 45-49).

Fourthly, because Bickford fails to teach an input buffer and an external signal path, Bickford also fails to teach coupling the first external signal path to the input buffer. Rather, AGP graphics accelerators 118, 122 are both coupled to the same AGP 110. (Id). Bickford teaches against the claims because Bickford teaches coupling the first external signal path to the first internal signal path. Again, rather than teaching coupling the first external signal path to the input buffer, Bickford is directed to a completely different problem and does not address the problems sought to overcome. For example, the Bickford reference is silent as to addressing echoes or signal reflections on transmission lines from expansion slots for an external graphics controller card and in fact, teaches away from addressing the problem since all embodiments appear to be shown with the AGP bus 110 being coupled directly to the AGP add-in card connector or to the AGP controller. In fact, the Bickford reference teaches enabling and disabling the AGP graphics accelerators 118, 122 and therefore uses a completely different approach from that claimed by Applicants. The Bickford reference suffers from the same problems described in Applicants' "Background of the Invention" section since the expansion slot AGP bus lines of Bickford are not isolated, but instead are coupled to the AGP 110 as with conventional configurations. In contrast, Applicants' invention addresses the problem of echoes or signal reflections from an expansion slot that can interfere with on chip graphics controllers' reception of signals. Accordingly, Bickford teaches away from the claims.

Fifthly, the Office Action acknowledges that Bickford does not disclose the claimed input buffer and hence the corresponding combination of structure with respect to the selector circuit and first internal circuit is also not disclosed. The Office Action takes official notice that it is common practice to allegedly use an input buffer with the AGP as claimed. Applicants respectfully note, as stated above, that Bickford teaches away from using Applicants' claimed input buffer by showing that the AGP bus 110 and the expansion slot 118 or onboard AGP graphics adaptor 122 are directly coupled. In fact, Bickford uses a completely different approach. As previously stated, Bickford teaches a conventional bus architecture coupled to peripheral devices and enabling and disabling the peripheral devices, such as AGP graphics accelerators 118, 122. As a result, Bickford teaches against the use of a first external path, an input buffer, and a selector circuit as previously stated. In fact, Bickford teaches the common practice of a conventional bus architecture coupled to peripheral devices and enabling and disabling the peripheral devices. This common practice teaches against the claims.

Consequently, the assertion that the common practice is to use an input buffer with the AGPs as claimed is unsupported and incorrect especially in view of the teachings of Bickford as cited. As a result, the assertion that the common practice is to use an input buffer with the AGPs as claimed is improper and therefore a *prima facie* case of obviousness is not established. If the Examiner maintains such an assertion, the Applicants respectfully challenge an assertion that it is common practice to 1) include an input buffer in an AGP as claimed, 2) include a first external path as claimed, and 3) include a selector circuit as arranged in the claims. As such, Applicants respectfully request a showing of such an assertion under MPEP 2112.

Sixthly, applicants also respectfully submit that there is no motivation other than Applicants' own specification, to combine an input buffer as claimed to an external signal path and selector as claimed. Therefore, the Office Action fails to establish a *prima facie* case of obviousness. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

As to claim 21, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that this claim requires, among other things, a bus bridge signal from an internal bus bridge and receiving, by an internal circuit, the bus bridge signal and further that an internal I/O circuit prevents signals from any external circuit from reaching the internal circuit. Again, as noted above, Bickford does not teach or suggest an internal I/O circuit that prevents signals from an external circuit from reaching an internal circuit, but in fact allows all external signals to pass to the AGP bus connected to the internal circuit. Instead, Bickford, as previously stated, teaches enabling and disabling the AGP graphics accelerators. Accordingly, this claim is also believed to be in condition for allowance.

As to claim 29, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that Bickford does not teach an integrated bus bridge graphics unit coupled to memory that includes an internal circuit operably configured to avoid signals from an external graphics bus. Instead, Bickford, as previously stated, teaches enabling and disabling the AGP graphics accelerators. Since Bickford teaches that the internal graphics bus is coupled directly to the external slot and to the internal AGP graphics chip (See FIG. 3), no external graphics bus is taught by Bickford. Bickford simply controls the receipt of a FRAME #

signal from the PCI bus to either of the two graphics controllers to enable or disable one of the two graphics controllers to operate. As such, this claim includes new and non-obvious subject matter and is also believed to be in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter and are also allowable. For example, as to claim 2, it is alleged that the Bickford reference discloses an output buffer (structure 170) and provides a second internal signal via the first external signal path. The Office Action admits that Bickford does not disclose, among other things, a separate second internal signal path for conveying signal to the output buffer. The Office Action, however, alleges that duplication of working parts of the device which are normally formed in two pieces is well known and that routine skill in the computer art would only be needed to add an additional internal signal path and to integrate the external output path and external input path into one external path. Applicants respectfully note that since Bickford does not describe a first external signal path, Bickford fails to describe the output buffer is operative to receive a second internal signal via the second internal path and to provide the second internal signal via the first external signal path in claim 2. Accordingly, such a combination of internal circuit, input buffer, output buffer and selector circuit is not taught or suggested by the cited references. Further, as stated above, the references teach against such a combination as claimed.

As to claim 20, the claim requires, among other things, that the input buffer is inoperable to provide the external signal from the first external signal path to the first internal circuit and that the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit. This isolation is not taught or suggested by Bickford and as such, this claim is also believed to be in condition for allowance.

Accordingly, Applicant respectfully submits that the Claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: Themi Anagnos
Themi Anagnos
Registration No. 47,888,

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VEDDER, PRICE, KAUFMAN &
KAMMHOLZ
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005